

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Peter J. Zdebel
FILED: Concurrently Herewith
FOR: HIGH ENERGY ESD STRUCTURE AND METHOD
Date: 12/29/2003

DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.56

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

SIR:

It is respectfully requested that the prior art listed on FORM PTO-1449 be considered in the examination of the subject application and made of record therein. A copy of the listed prior art is enclosed herewith.

No representation is made or intended that the listed prior art enclosed herewith is material to patentability of the subject patent application.

No representation is made or intended that a search has been made or that no better prior art than that listed is available.

Respectfully submitted,
Peter J. Zdebel et al



ON Semiconductor
Intellectual Property Dept.
P.O. Box 62890 - A700
Phoenix, AZ 85062-2890

Kevin B. Jackson
Reg. #38,502
Phone: 602-244-5603
Fax: 602-244 3169

Customer #: 27255

Form PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use Several Sheets if Necessary)	ATTY. DOCKET NO.	SERIAL NO.
	Ons00535	
	APPLICANT Peter Zdebel et al	
	FILING DATE	GROUP
	Concurrently herewith	

REFERENCE DESIGNATION									U.S. PATENT DOCUMENTS					
EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
	AA													
	AB													
	AC													
	AD													
	AE													
	AF													
	AG													
	AH													
	AI													
	AJ													
	AK													
	AL													

FOREIGN PATENT DOCUMENTS													
Examiner Initial		Document #								Date	Country	Class/subclass	Translation Yes - No
	AM												
	AN												
	AO												
	AP												
	AQ												
	AR												

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)													
	AS		V. Vashchenko et al., "Comparison of ESD Protection Capability of Lateral BJT, SCR, and bi-directional SCR for Hi-Voltage BiCMOS Circuits," IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pages 181-184, September 29 - October 1, 2002.										
	AT		Haigang Feng, et al., "An ESD Protection Circuit for Mixed-Signal ICs," IEEE 2001 Custom Integrated Circuits Conference, pages 493-496, May 6-9, 2001.										
	AU		Ke Gong et al., "A Study of Parasitic Effects of ESD Protection on RF ICs," IEEE Transactions on Microwave Theory and Techniques, Vol. 50, No. 1, pages 393-402, January 2002.										
	AV		H.G. Feng et al., "Circular Under-Pad Multiple Mode ESD Protection Structure for ICs," Electronics Letters, Vol. 38, No. 11, pages 511-513, May 23, 2002.										
	AW		Guang Chen et al., "A Systematic Study of ESD Protection Structures for RF ICs," 2003 IEEE Radio Frequency Integrated Circuits Symposium, pages 347-350, June 8-10, 2003.										

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.